CPE241 Digital Logic Design

Midterm Exam

Instructor: Dr. Babar Mansoor
Max Marks: 25
Time Allowed : 70 Minutes

Class: BCE2R
Date: 15-11-22

Q(1) [CLO1,C2](4 Marks)

(a) (2 Marks) Convert $(11.375)_{10}$ to binary. $(1011.011)_2$

(b) (2 Marks) Compute $64_{10} - 100_{10}$ using 8-bit 2's complement addition. Provide the 8-bit result and indicate whether twos complement overflow occurred. Check your work by converting the 8-bit result back to decimal.

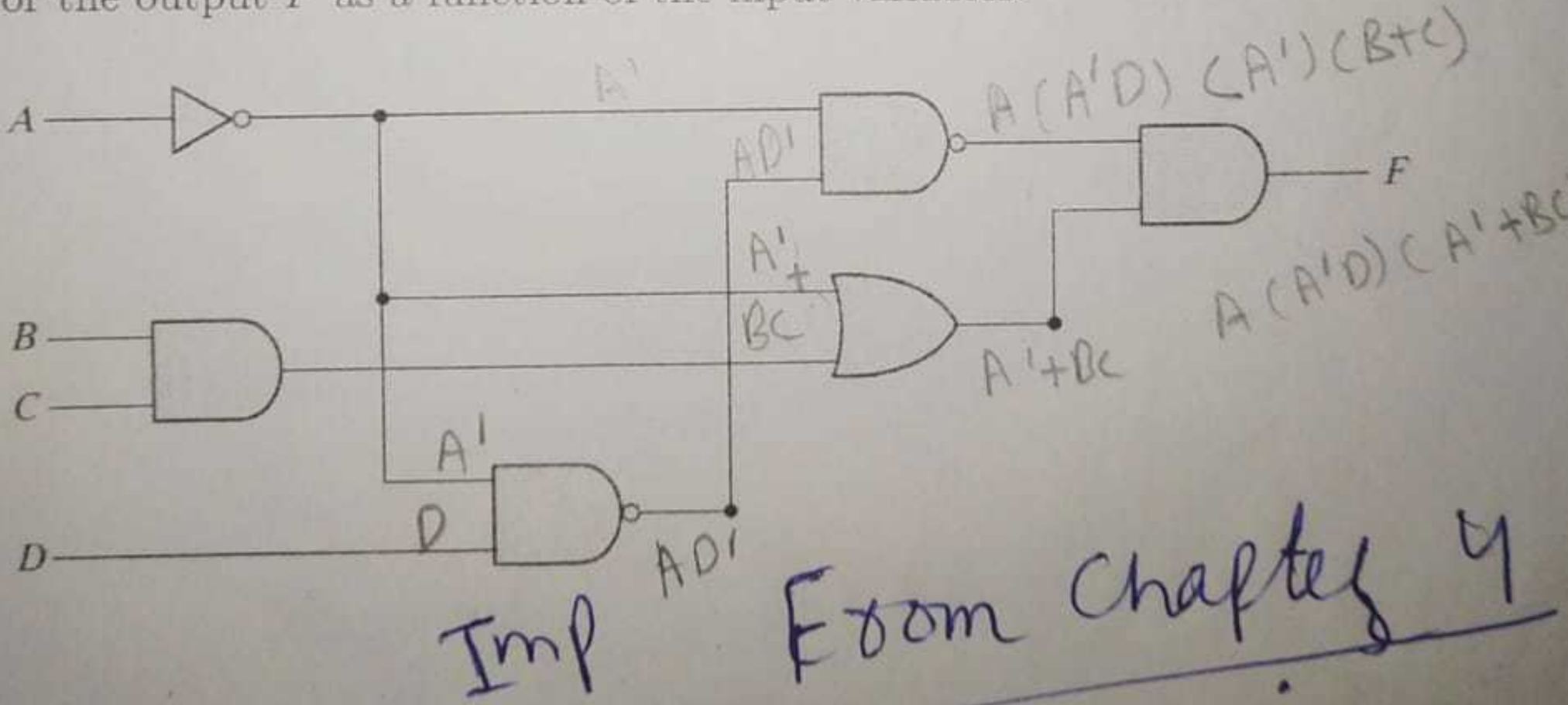
Q(2) [CLO2,C3](4 Marks)

(a) (2 Marks) Implement $F = xy + x'y' + y'z$ using NAND gates only.

(b) (2 Marks) Express $F(A, B, C, D) = \prod(3, 5, 7)$ in sum-of-minterms form. $A'B'CD + A\bar{B}C'D + A'BCD$.

Q(3) [CLO3,C4](4 Marks)

Consider the circuit shown in figure below. Analyze the circuit to obtain the Boolean expression for the output F as a function of the input variables.



Imp From chapter 4 exercise

Q(4) [CLO4,C6](5 Marks)

A logic circuit realizing the function f has four inputs a, b, c, d. The three inputs a, b, and c are the binary representation of the digits 0 through 7 with a being the most significant bit. The input d is an odd-parity bit; that is, the value of d is such that a, b, c, and d always contains an odd number of 1s. (For example, the digit 1 is represented by $abc = 001$ and $d = 0$, and the digit 3 is represented by $abcd = 0111$.) The function f has value 1 if the input digit is a prime number. (A number is prime if it is divisible only by itself and 1; 1 is considered to be prime, and 0 is not). Realize the Boolean function f with minimum, number of logic gates.

A'B+C

Q(5) [CLO4,C6](5 Marks)

Design an 8-to-1 multiplexer circuit using 2-to-1 multiplexers.

Q(6) [CLO4,C6](3 Marks)

Design a 3-bit binary adder/subtractor circuit with overflow detection.

——— The End ———-