COMSATS University Islamabad (CUI), Islamabad
Department of Electrical & Computer Engineering

CPE241 Digital Logic Design
Final Exam Fall 2024

Instructor: Dr. Babar Mansoor
Max Marks: 50
Time Allowed: 03 Hours

Class: BCE 3B
Date: 18-01-2025

Q(1)[CLO3](5 Marks)
Analyze the following circuit shown in Figure 1 to express the functions F_1 and F_2 in terms of the inputs A, B and C. What is the relationship between F_1 and F_2?

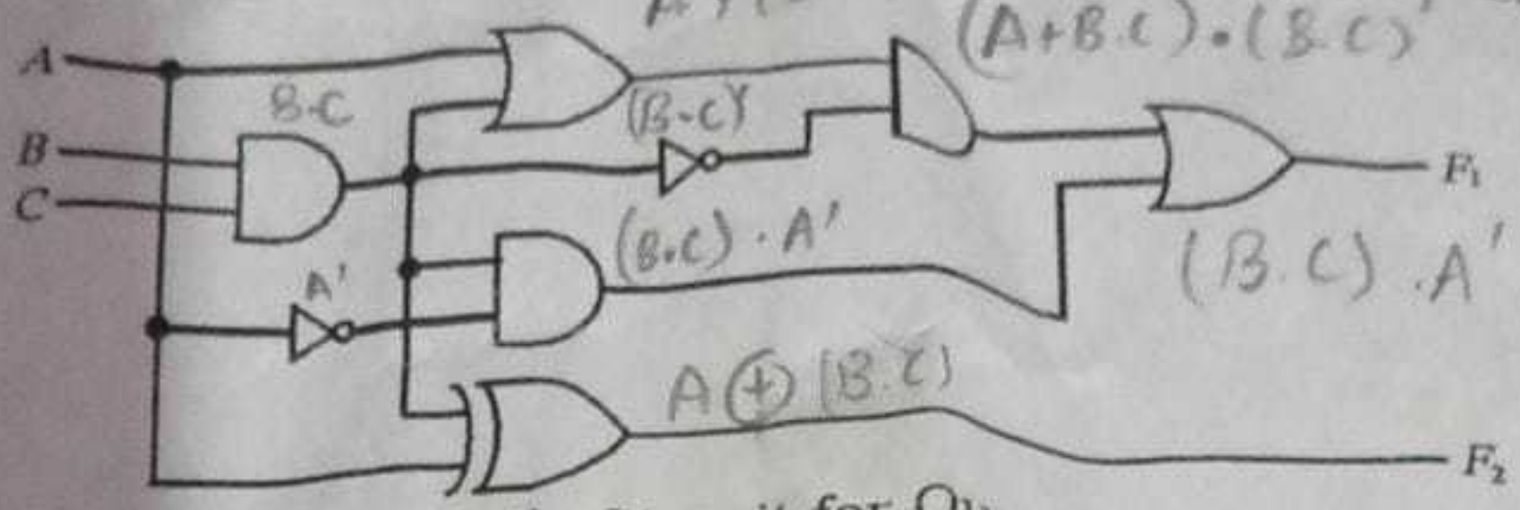

Figure 1. Circuit for Question 1

Q(2)[CLO4](10 Marks)

a) **(5 Marks)** Design a combinational circuit with minimum number of gates to convert a 3-bit input binary number into its equivalent Gray code.

b) **(5 Marks)** Design a 3-bit magnitude comparator circuit for two binary numbers $A = a_2a_1a_0$ and $B = b_2b_1b_0$ as inputs. The required circuit has three outputs namely **EQ** (if A==B), **GT** (if A>B) and **LT** (if A<B).

Q(3) [CLO3](5 Marks)
Analyze the behavior of a positive edge triggered JK flip flop by deriving its state transition table, next state equations and state diagram. Also write down the excitation table of a JK flip flop.

Q(4)[CLO3] (10 Marks)
Consider the sequential circuit shown in **Figure 2**. Analyze this circuit by deriving:

1) State transition and output equations,
2) State transition table,
3) State diagram.
4) Draw a timing diagram for the input sequence X=0110010

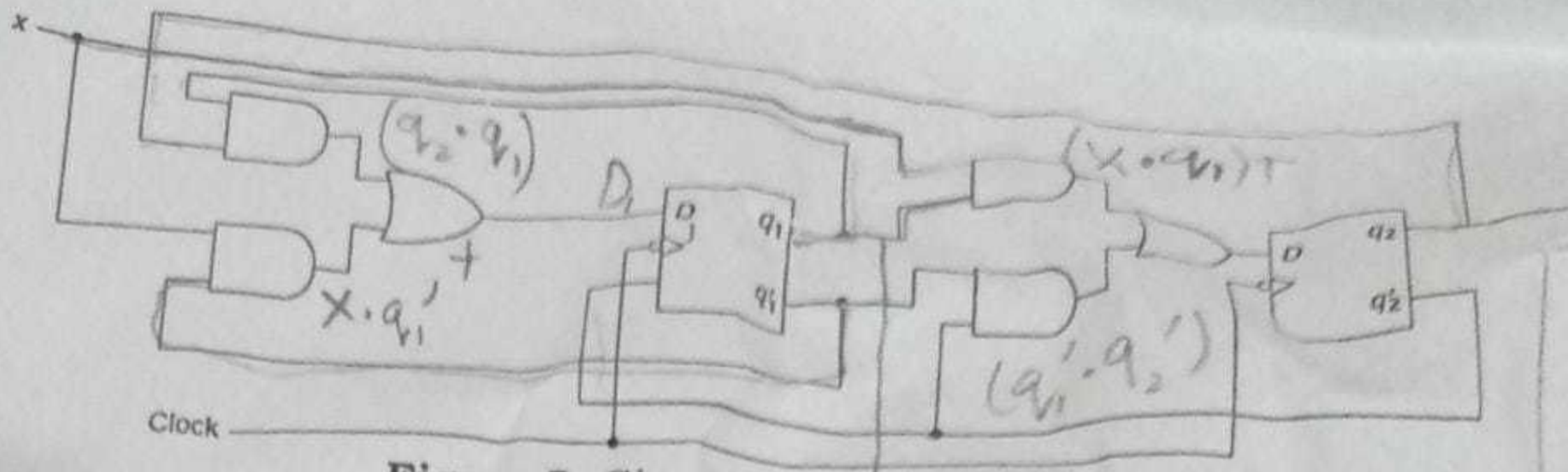

Figure 2. Circuit for Question 4

Q(5) [CLO4](10 Marks)

Design a Mealy system whose output is 1 for every third 1 input (**not necessarily consecutive**). For example, if X is the input and Z is the output of the detector, then a sample pattern of X and Z is shown below:

X	0	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1	0	1
Z	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0

Design the circuit using D type flip flops.

Q(6) [CLO4](10 Marks)

a) **(7 Marks)** Design a 2-bit Up/Down counter with two inputs: **E** (Enable) and **U** (Up).If **E = 0** then counter remains in the same state (regardless of U) If **EU = 11** then count up from 0 to 3, then back to 0 If **EU = 10** then count down from 3 down to 0, then back to 3. The circuit should be designed using T flip flops.

b) **(3 Marks)** Design a bit-serial adder to add two 4-bit binary numbers A and B and store the sum in a register. Use D flip flops.