COMSATS University Islamabad

Islamabad Campus
Computer Science Department
Final Exam

Class: BCS-2B
Subject: Digital Logic Design (EEE-241)
Instructor: Fahad Sharief

Date: Jan 03, 2024
Time Allowed: 180 minutes
Marks: 50

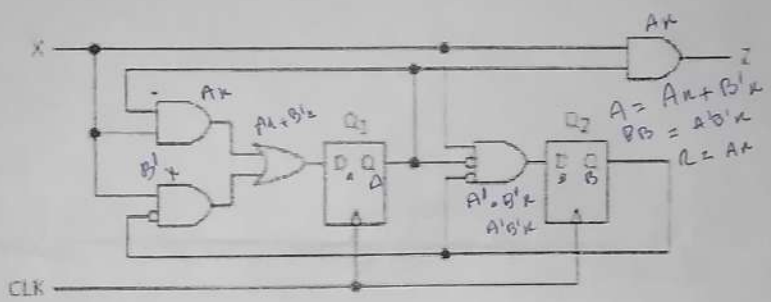
Instructions: -Attempt all questions

Q No.1) **(7 marks)**

Design a clocked sequential circuit using synthesis with D flip flops, such that it detects the three most significant bits of your registration number binary value. (For example registration no. 097 binary value is 1 1 0 0 0 0 1 and the underline three bits are MSB i.e. 1 1 0).

Q No.2) **(7+2=9 marks)**

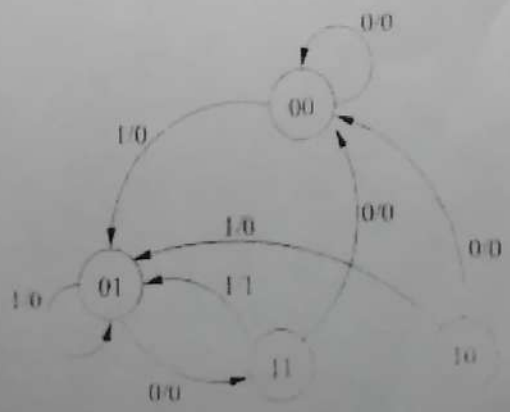
a. Derive the state table and draw state diagram for the circuit given in Figure below.
b. Is this a Mealy or a Moore Finite Machine and Why?



Q No.3) **(2+8=10 marks)**

Consider the following state diagram given in Figure below for synchronous circuit with one input "X" and one output "Z".

a. From the state diagram Analyze what the circuit is doing.
b. Analyze state diagram and Design its circuit implementation using JK Flip Flops



P.T.O

Q No.4) **(5+5=10 marks)**

a. Design a 16-to-1 multiplexer using 2-to-1 multiplexers. Use as many MUX of 2-to-1 you need.

b. Design a Full adder circuit by using multiple 2 to 4 line decoders.

Q No.5) **(3+4=7 marks)**

a. Design a logic circuit with minimum numbers of gates represented by the truth table given below in sum of Product form and product of sum form.

x	y	z	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

b. For the Boolean Function $F\ (ABCD) = ABC' + BC'D' + CD + A'B$, Implement the simplified expression with NOR gate only.

Q No.6) **(7 marks)**

What are shift registers? Draw the block diagram to explain its application of serial to parallel data conversion. Explain the working with an appropriate timing diagram.

********** GOOD LUCK **********